U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
*	A	US-6,035,107	03-2000	Kuehlmann et al.	716/1
*	B	US-6,799,307	09-2004	Lipton et al.	716/5
*	C	US-2004/0177332	09-2004	Pandey et al.	716/005
*	D	US-5,249,133	09-1993	Batra	716/5
*	E	US-5,867,396	02-1999	Parlour	716/18
*	F	US-6,473,881	10-2002	Lehner et al.	716/2
*	G	US-6,591,402	07-2003	Chandra et al.	716/5
*	H	US-2004/0243949	12-2004	Wang et al.	716/004
*	I	US-2005/0114805	05-2005	Novakovsky et al.	716/004
*	J	US-2005/0143966	06-2005	McGaughy	703/003
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	Barke et al., "A Network Comparison Algorithm for Layout Verification of Integrated Circuits", April 1984, Transactions on, Volume 3, Issue 2, Page(s):135 - 141
	V	Piriyakumar et al., "A novel isomorphism based on nearest neighbours for efficient graph matching algorithm", Dec. 2002, Control, Automation, Robotics and Vision, 7th International Conference on□□Volume 2, 2-5 Page(s):722 - 727 vol.2
	W	Fan et al., "Structural isomorphism of pictorial graphs", 9-12 April 1989, Southeastcon '89. Proceedings. 'Energy and Information Technologies in the Southeast'., IEEE, Page(s):628 - 633 vol.2
	X	Rangarajan et al., "A Lagrangian relaxation network for graph matching", Nov. 1996 , Neural Networks, IEEE Transactions on, Volume 7, Issue 6, Page(s):1365 - 1381

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
	A	US-			
	B	US-			
	C	US-			
	D	US-			
	E	US-			
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	Kupeev et al., "On shape similarity", 9-13 Oct. 1994, Image Processing., Proceedings of the 12th IAPR International Conference on, Volume 1, Page(s):227 - 231 vol.1
	V	Takashima et al., "A circuit comparison system with rule-based functional isomorphism checking", 12-15 June 1988, Design Automation Conference, Proceedings., 25th ACM/IEEE,☐☐Page(s):512 - 516
	W	Rubanov et al., "SubIslands: the probabilistic match assignment algorithm for subcircuit recognition", Jan. 2003, Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on, Volume 22, Issue 1, Page(s):26 - 38
	X	Abadir et al., "An improved layout verification algorithm (LAVA)", 12-15 March 1990, Design Automation Conference, EDAC. Proceedings of the European, Page(s):391 - 395

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

		Application/Control No. 10/616,215	Applicant(s)/Patent Under Reexamination MEDING, UWE	
Notice of References Cited		Examiner Helen Rossoshek	Art Unit 2825	Page 3 of 3

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
	A	US-			
	B	US-			
	C	US-			
	D	US-			
	E	US-			
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	Terem et al., "Pattern search in hierarchical high-level designs", 13-15 Dec. 2004, Electronics, Circuits and Systems, 2004. ICECS 2004. Proceedings of the 2004 11th IEEE International Conference on, Page(s):519 - 522
	V	Watanabe et al., "A New Automatic Logic Interconnection Verification System for VLSI Design", April 1983, Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on□□Volume 2, Issue 2, Page(s):70 - 82
	W	Ebeling et al., "Geminill: a second generation layout validation program", 7-10 Nov. 1988, Computer-Aided Design, Digest of Technical Papers., IEEE International Conference on, Page(s):322 - 325
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.